Application No. 10/735,489
October 10, 2005
Amendment responsive to Office Action of September 28, 2005

In the Claims:

Please amend the claims as indicated below:

1-5. (canceled)

6.(previously presented) A system comprising:

transistors adapted to operate as an SR flip-flop wherein each one of the transistors has an insulated gate and wherein the SR flip-flop is a SEUSSNor comprising:

a power node and four p type transistors named P2, P4, P6, and P8 wherein the sources of P2, P4, P6, and P8 are connected to the power node;

a ground node and eight n type transistors named N1, N2, N3, N4, N5, N6, N7, and N8 wherein the sources of N1, N2, N3, N4, N5, N6, N7, and N8 are connected to the ground node;

a p type transistor called P1 wherein the source of P1 is connected to the drain of P2;

a p type transistor called P3 wherein the source of P3 is connected to the drain of P4;

a p type transistor called P5 wherein the source of P5 is connected to the drain of P6;

a p type transistor called P7 wherein the source of P7 is connected to the drain of P8;

an S input connected to the gate of P1, the gate of N1, the gate of N5 and the gate of P5;

an R input connected to the gate of P3, the gate of N3, the gate of N7 and the gate of P7;

a Q2 node connected to the gate of P2, the gate of N6, the drain of N7, the drain of P7, and the drain of N8;

a Qbar node connected to the gate of P4, the gate of N8, the drain of N1, the drain of P1, and the drain of N2;

a Q node connected to the gate of P6, the gate of N2, the drain of N3, the drain of P3, and the drain of N4; and

a Qbar2 node connected to the gate of P8, the gate of N4, the drain of N5, the drain of P5, and the drain of N6.

7-10.(cancelled)

11.(previously presented) A system comprising:

transistors adapted to operate as an SR flip-flop wherein each one of the transistors comprises has an insulated gate and wherein the SR flip-flop is a SEUSSNand comprising:

a power node and eight p type transistors named P1, P2, P3, P4, P5, P6, P7, and P8 wherein the sources of P1, P2, P3, P4, P5, P6, P7, and P8 are connected to the power node;

a ground node and four n type transistors named N2, N4, N6, and N8 wherein the sources of N2, N4, N6, and N8 are connected to the ground node;

an n type transistor called N1 wherein the source of N1 is connected to the drain of N2;

an n type transistor called N3 wherein the source of N3 is connected to the drain of N4;

an n type transistor called N5 wherein the source of N5 is connected to the drain of N6;

an n type transistor called N7 wherein the source of N7 is connected to the drain of N8;

an S input connected to the gate of P1, the gate of N1, the gate of N5 and the gate of P5;

an R input connected to the gate of P3, the gate of N3, the gate of N7 and the gate of P7;

a Qbar2 node connected to the gate of P2, the gate of N6, the drain of P7, the drain of N7, and the drain of P8;

a Q node connected to the gate of P4, the gate of N8, the drain of N1, the drain of P1, and the drain of P2;

a Qbar node connected to the gate of P6, the gate of N2, the drain of N3, the drain of P3, and the drain of P4; and

a Q2 output node connected to the gate of P8, the gate of N4, the drain of N5, the drain of P5, and the drain of P6.

12-15.(cancelled)

16.(previously presented) The system of claim 6 further comprising at least two more SR flip flops and a voting circuit such that the circuit output is the majority output of all of the SR flip-flops.

17.(currently amended) The system of claim 16 wherein the voting circuit is a TRed2 circuit. 6 further comprising:

a two input NAND gate called G1 wherein the first input of G1 is connected to a TRed2 R input node and the output of G1 is connected to the S input;

a two input NAND gate called G2 wherein the first input of G2 is connected to a TRed2 S input node and the output of G2 is connected to the second input of G1;

a two input NAND gate called G3 wherein the first input of G3 is connected to the TRed2 S input node and the output of G3 is connected to the R input;

a two input NAND gate called G4 wherein the first input of G4 is connected to the TRed2 R input node and the output of G4 is connected to the second input of G3;

an SR flip-flop called SR2 wherein the S input of SR2 is connected to the output of G1 and the R input of SR2 is connected to the output of G3;

an SR flip-flop called SR3 wherein the S input of SR3 is connected to the output of G1 and the R input of SR3 is connected to the output of G3;

a three input NAND gate called G5 wherein the first input of G5 is connected to either the Q node or the Q2 node, the second input of G5 is connected to the Q output of SR2, and the third input of G5 is connected to the Q output of SR3;

_____ a three input NAND gate called G6 wherein the first input of G6 is connected to either the Qbar node or the Qbar2 node, the second input of G6 is connected to the Qbar output of SR2, and the third input of G6 is connected to the Qbar output of SR3;

_____ a two input NAND gate called G7 wherein the first input of G7 is connected to either the Q node or the Q2 node and the second input of G7 is connected to the Q output of SR2;

_____ a two input NAND gate called G8 wherein the first input of G8 is connected to either the Q node or the Q2 node and the second input of G8 is connected to the Q output of SR3;

_____ a two input NAND gate called G9 wherein the first input of G9 is connected to the Q output of SR2 and the second input of G9 is connected to the Q output of SR3;

_____ a three input NAND gate called G10 wherein the first input of G10 is connected to the output of G7, the second input of G10 is connected to the output of G8, the third input of G10 is connected to the output of G9, and the output of G10 is connected to a TRed2 Q output node;

_____ an inverter called I1 wherein the input of I1 is connected to the TRed2 Q output node and the output of I1 is connected to a TRed2 Qbar output node;

_____ a two input NAND gate called G11 wherein the first input of G11 is connected to the output of G5 and the second input of G11 is connected to the output of G10 and the output of G11 is connected to the second input of G4; and

_____ a two input NAND gate called G12 wherein the first input of G12 is connected to the output of G6 and the second input of G12 is connected to the output of I1 and the output of G12 is connected to the second input of G2.

18.(previously presented) The system of claim 6 further comprising at least two more SR flip flops and a correction circuit such that the circuit output is the corrected output of all of the SR flip-flops.

19.(currently amended) The system of claim ~~18 wherein the voting circuit is a TRed1 circuit.~~6 further comprising:

_____ a two input NAND gate called G1 wherein the first input of G1 is connected to a TRed1 R input node and the output of G1 is connected to the S input;

_____ a two input NAND gate called G2 wherein the first input of G2 is connected to a TRed1 S input node and the output of G2 is connected to the second input of G1;

_____ a two input NAND gate called G3 wherein the first input of G3 is connected to the TRed1 S input node and the output of G3 is connected to the R input;

_____ a two input NAND gate called G4 wherein the first input of G4 is connected to the TRed1 R input node and the output of G4 is connected to the second input of G3;

_____ an SR flip-flop called SR2 wherein the S input of SR2 is connected to the output of G1 and the R input of SR2 is connected to the output of G3;

_____ an SR flip-flop called SR3 wherein the S input of SR3 is connected to the output of G1 and the R input of SR3 is connected to the output of G3;

_____ a TRed1 Q node connected to either the Q node or the Q2 node;

_____ a TRed1 Qbar node connected to either the Qbar node or the Qbar2 node;

a two input NAND gate called G11 wherein the first input of G11 is connected to the Q output of SR2 and the second input of G11 is connected to the Q output of SR3;

a two input NAND gate called G12 wherein the first input of G12 is connected to the Qbar output of SR2 and the second input of G12 is connected to the Qbar output of SR3;

a two input NAND gate called G13 wherein the first input of G13 is connected to the output of G11 and the second input of G13 is connected to the output of G12;

a two input NAND gate called G5 wherein the first input of G5 is connected to the TRed1 Q node and the second input of G5 is connected to the output of G13;

a two input NAND gate called G6 wherein the first input of G6 is connected to the TRed1 Qbar node and the second input of G6 is connected to the output of G11;

a two input NAND gate called G7 wherein the first input of G7 is connected to the output of G5, the second input of G7 is connected to the output of G6 and the output of G7 is connected to the second input of G2;

a two input NAND gate called G8 wherein the first input of G8 is connected to the TRed1 Qbar node and the second input of G8 is connected to the output of G13;

a two input NAND gate called G9 wherein the first input of G9 is connected to the TRed1 Q node and the second input of G9 is connected to the output of G12; and

a two input NAND gate called G10 wherein the first input of G10 is connected to the output of G8, the second input of G10 is connected to the output of G9 and the output of G10 is connected to the second input of G4.

20.(previously presented) The system of claim 11 further comprising at least two more SR flip flops and a voting circuit such that the circuit output is the majority output of all of the SR flip-flops.

21.(currently amended) The system of claim 20 wherein the voting circuit is a TRed2 circuit.11 further comprising:

a two input NAND gate called G1 wherein the first input of G1 is connected to a TRed2 R input node and the output of G1 is connected to the S input;

a two input NAND gate called G2 wherein the first input of G2 is connected to a TRed2 S input node and the output of G2 is connected to the second input of G1;

a two input NAND gate called G3 wherein the first input of G3 is connected to the TRed2 S input node and the output of G3 is connected to the R input;

a two input NAND gate called G4 wherein the first input of G4 is connected to the TRed2 R input node and the output of G4 is connected to the second input of G3;

an SR flip-flop called SR2 wherein the S input of SR2 is connected to the output of G1 and the R input of SR2 is connected to the output of G3;

an SR flip-flop called SR3 wherein the S input of SR3 is connected to the output of G1 and the R input of SR3 is connected to the output of G3;

a three input NAND gate called G5 wherein the first input of G5 is connected to either the Q node or the Q2 output node, the second input of G5 is connected to the Q output of SR2, and the third input of G5 is connected to the Q output of SR3;

a three input NAND gate called G6 wherein the first input of G6 is connected to either the Qbar node or the Qbar2 node, the second input of G6 is connected to the Qbar output of SR2, and the third input of G6 is connected to the Qbar output of SR3;

a two input NAND gate called G7 wherein the first input of G7 is connected to either the Q node or the Q2 output node and the second input of G7 is connected to the Q output of SR2;

a two input NAND gate called G8 wherein the first input of G8 is connected to either the Q node or the Q2 output node and the second input of G8 is connected to the Q output of SR3;

a two input NAND gate called G9 wherein the first input of G9 is connected to the Q output of SR2 and the second input of G9 is connected to the Q output of SR3;

a three input NAND gate called G10 wherein the first input of G10 is connected to the output of G7, the second input of G10 is connected to the output of G8, the third input of G10 is connected to the output of G9, and the output of G10 is connected to a TRed2 Q output node;

an inverter called I1 wherein the input of I1 is connected to the TRed2 Q output node and the output of I1 is connected to a TRed2 Qbar output node;

a two input NAND gate called G11 wherein the first input of G11 is connected to the output of G5 and the second input of G11 is connected to the output of G10 and the output of G11 is connected to the second input of G4; and

_____ a two input NAND gate called G12 wherein the first input of G12 is connected to the output of G6 and the second input of G12 is connected to the output of I1 and the output of G12 is connected to the second input of G2.

22.(previously presented) The system of claim 11 further comprising at least two more SR flip flops and a correction circuit such that the circuit output is the corrected output of all of the SR flip-flops.

23.(currently amended) The system of claim ~~22 wherein the voting circuit is a TRed1 circuit.~~11 further comprising:

_____ a two input NAND gate called G1 wherein the first input of G1 is connected to a TRed1 R input node and the output of G1 is connected to the S input;

_____ a two input NAND gate called G2 wherein the first input of G2 is connected to a TRed1 S input node and the output of G2 is connected to the second input of G1;

_____ a two input NAND gate called G3 wherein the first input of G3 is connected to the TRed1 S input node and the output of G3 is connected to the R input;

_____ a two input NAND gate called G4 wherein the first input of G4 is connected to the TRed1 R input node and the output of G4 is connected to the second input of G3;

_____ an SR flip-flop called SR2 wherein the S input of SR2 is connected to the output of G1 and the R input of SR2 is connected to the output of G3;

_____ an SR flip-flop called SR3 wherein the S input of SR3 is connected to the output of G1 and the R input of SR3 is connected to the output of G3;

a TRed1 Q node connected to either the Q node or the Q2 output node;

a TRed1 Qbar node connected to either the Qbar node or the Qbar2 node;

a two input NAND gate called G11 wherein the first input of G11 is connected to the Q output of SR2 and the second input of G11 is connected to the Q output of SR3;

a two input NAND gate called G12 wherein the first input of G12 is connected to the Qbar output of SR2 and the second input of G12 is connected to the Qbar output of SR3;

a two input NAND gate called G13 wherein the first input of G13 is connected to the output of G11 and the second input of G13 is connected to the output of G12;

a two input NAND gate called G5 wherein the first input of G5 is connected to the TRed1 Q node and the second input of G5 is connected to the output of G13;

a two input NAND gate called G6 wherein the first input of G6 is connected to the TRed1 Qbar node and the second input of G6 is connected to the output of G11;

a two input NAND gate called G7 wherein the first input of G7 is connected to the output of G5, the second input of G7 is connected to the output of G6 and the output of G7 is connected to the second input of G2;

a two input NAND gate called G8 wherein the first input of G8 is connected to the TRed1 Qbar node and the second input of G8 is connected to the output of G13;

a two input NAND gate called G9 wherein the first input of G9 is connected to the TRed1 Q node and the second input of G9 is connected to the output of G12; and

a two input NAND gate called G10 wherein the first input of G10 is connected to the output of G8, the second input of G10 is connected to the output of G9 and the output of G10 is connected to the second input of G4.

24-28.(cancelled)